Remarks

Upon entry of the foregoing amendment, claims 1-19 and 40-48 are pending in the application, with claims 1 and 11 being the independent claims. Claims 1 and 11 are sought to be amended for clarification purposes as discussed below. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections Under 35 U.S.C. § 112

Claims 1-19 and 40-48 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly be indefinite. According to the Examiner, the limitation "the absolute value of each of the at least one of the plurality of transformed coordinates" renders claims 1 and 11 indefinite. The Examiner also alleges that the phrase "a single comparison operation" can not be understood by a person skilled in relevant art after reading the specification. Finally, the Examiner alleges that there is no antecedent basis for the phrase "the absolute value of each of" recited in claims 1 and 11.

Applicants have amended claims 1 and 11 to clarify the claims. Reconsideration and withdrawal of this rejection are respectfully requested.

Rejections Under 35 U.S.C. § 103

Claims 1-19 and 40-48 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,720,019 ("Koss") in view of U.S. Patent No. 6,169,554 ("Deering") and MIPS R4000 Microprocessor User's Manual ("Heinrich"). In addition,

claims 1 and 11 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koss in view of U.S. Patent No. 6,298,365 ("Dubey") and Heinrich.

Generally speaking, the claimed invention relates to a processor having an expanded instruction set that facilitates 3D graphics processing. One of the instructions of the expanded instruction set is a CABS instruction.

As described in the present application (e.g., beginning on page 88, line 1), in 3-D graphics applications a clip test is performed to determine which primitives, or parts of primitives, will appear in a displayed graphics image. The clip test can be performed using the CABS instruction to compare the absolute values of transformed coordinate values (e.g., x', y', z') for each vertex against the absolute values of the standard viewing planes (e.g., w'). The CABS instruction performs magnitude compares (e.g., $|x'| \leq |w'|$), which replace the conventional two-step inequality evaluations ($x \leq w$ and $x \geq -w$) that are used to implement clip testing in conventional processors.

In paired-single format, the CABS instruction provides the capability for performing two magnitude compares and testing up to four view volume edges in one clock cycle. As described in the present application, in a paired-single format, the CABS instruction can compare the absolute values of a first data set (e.g., x' and y' representing transformed vertex coordinates) with the absolute values of a second data set (e.g., w' and w' representing viewing planes or, more specifically, two view volume edges of a three-dimensional volume) to clip test four view volume edges in a single operation. (See, e.g., Table 3 on page 90 and the description thereof starting on page 91 of the present application.) This is illustrated by the pseudocode of Table 3. Because the CABS instruction can be executed in a single clock cycle, four view volume edges can be compared in a single cycle.

In accordance with the disclosure of the present application, claim 1 recites:

> 1. In a processor, a method for performing computer graphics view volume clipping comparisons to determine if a vertex is located within a specified view volume, the method comprising:
>
> transforming a plurality of coordinates representing the vertex into a plurality of transformed coordinates; and
>
> using a floating point magnitude compare instruction to
>
> determine an absolute value of at least one of the plurality of transformed coordinates and an absolute value that represents, for each respective at least one transformed coordinate, opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate, and
>
> perform a magnitude comparison between the absolute value of the at least one of the plurality of transformed coordinates and the absolute value of the corresponding view volume edges, wherein comparison results for at least two view volume edges are obtained.

Independent claim 11 recites similar features.

The rejection of claims 1-19 and 40-48 under 35 U.S.C. § 103(a) is improper. Koss relates to a graphics processing circuit for use in a graphics accelerator. (See abstract of Koss.) The graphics accelerator of Koss is not a processor having an expanded instruction set that facilitates 3-D graphics processing. For example, nowhere does Koss disclose or suggest "a floating point magnitude compare instruction" as described and claimed in the present application.

As noted by the Examiner, the graphics accelerator of Koss includes a clipping preprocessor circuit that uses a comparator. The comparator "can be a floating point comparator." (See col. 2, ln. 42 of Koss.) FIG. 4 of Koss actually shows that two floating point comparators are used. As described by Koss at column 8, lines 42-54:

> Each of the floating point comparators 206, 208 compares the two floating point numbers it receives and provides a signal that indicates which one is larger. In particular, the first floating

> point comparator 206 provides a logic high signal (binary one) on a maximum output line 210 if the value it receives from the vertex coordinate register 202 is higher than the value it receives from the maximum register 200. Conversely, the second floating point comparator 208 provides a logic high signal on a minimum output line 212 if the value it receives from the vertex coordinate register is less than the value it receives from the minimum register 204.

This description in Koss is suggestive of the two-step inequality evaluations ($x \leq w$ and $x \geq -w$) used to implement clip testing in a conventional processor. It does not make obvious the floating point magnitude compare instruction disclosed and claimed in the present application. Koss also states that:

> In order to operate on signed values, the comparators are implemented as magnitude comparators with additional circuitry. In particular, referring also to FIG. 5, the second comparator 208 includes a magnitude comparator 213 that has a first input port operatively connected to the second output bus 203 which is from the output port of the vertex coordinate register 202. The magnitude comparator has a second input port operatively connected to the third output bus 205, which is from the output port of the minimum clipping extent register 204.

(See col. 8, ln. 62 - col. 9, ln. 4 of Koss.) This statement by Koss, however, does not change the overall operation of the clipping preprocessor circuit of Koss. Deering, Heinrich, and Dubey do not overcome the deficiencies of Koss.

For at least the reasons provided herein, claims 1 and 11 are patentable over the applied references. Claims 2-10, 12-19, and 40-48 depend from claim 1 or 11, either directly or indirectly, and are patentable for at least the same reasons as claims 1 and 11, and further for the specific features they recite. Reconsideration and withdrawal of this rejection of claims 1-19 and 40-48 are respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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